AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-15 (Canceled)

16. (Currently Amended) A process for the fabrication of contact pads of electronic chips [[from]] in a semiconductor wafer comprising, ~~on its~~on a front face of the wafer, a thin active layer of semiconductor material, the process comprising steps of:

formatting of etched layers on the active layer;

bonding the wafer by its front face onto a support substrate;

and thereafter thinning down of the semiconductor wafer ~~via its~~via a backside opposite the front face, [[;]]

[[the]] depositing ~~and etching~~at least one metal layer ~~of layers of material on its~~on the backside thus thinned, and etching at least one contact pad in said metal layer,

said process including the following steps:

etching ~~wherein~~ narrow ~~vertical~~ trenches ~~are etched~~ into the ~~wafer by its front face~~thin active layer, before the bonding operation, these trenches extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation,

filling the space opened by said trenches ~~being filled~~ with a conducting material isolated from the active layer, thus ~~and~~ forming conducting vias between the front face and the backside of the thinned ~~layer.~~wafer, [[;]]

wherein said trenches comprise a series of parallel trenches located under the contact pad, the contact pad being in electrical contact with the conducting material in said parallel trenches.

17. (Previously Presented) The process as claimed in claim 16, wherein the trenches are formed before other deposition and etching steps of electrically functional layers on the front face of the semiconductor wafer.

18. (Currently Amended) The process as claimed in claim 16, wherein ~~the~~ said trenches comprise at least one trench ~~takes~~ in the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face.

19. (Currently Amended) The process as claimed in claim 16, wherein ~~the~~ said at least one metal layer is deposited onto the backside of the wafer after thinning, this layer being connected, by conducting vias formed within at least one narrow trench, to at least one conducting layer formed, prior to bonding the wafer onto the support substrate, on the front face of the wafer.

20. (Currently Amended) The process as claimed in claim [[19]] 16, wherein said electronic chips comprise at least one image sensor with a matrix of pixels and the said at least one metal layer comprises a pattern within the matrix of pixels~~is a photo-masking layer designed to prevent light impinging on photosensitive parts within an image sensor formed on the wafer~~.

21. (Previously Presented) The process as claimed in claim 16, wherein layers of color filters are deposited onto the backside of the wafer after bonding and thinning.

22. (Previously Presented) The process as claimed in claim 21, wherein, after deposition of the color filters, the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated.

23. (Currently Amended) The process as claimed in claim [[1]] 16, wherein the trenches have their internal walls coated with thin silicon oxide and are filled with polycrystalline silicon that is highly doped so as to be conducting.

24. (Canceled)

25. (Previously Presented) The process as claimed in claim 16, wherein the semiconductor wafer comprises a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.

26 -29 (Canceled)

30. (New) The process as claimed in claim 16, wherein said trenches comprise, for said at least one contact pad, a continuous trench completely surrounding said parallel trenches and surrounding a semiconductor region containing said parallel trenches, the contact pad being isolated from the conductive material filling said continuous trench.

31. (New) A process for the fabrication of contact pads of electronic chips in a semiconductor wafer comprising, on a front face of the wafer, a thin active layer of semiconductor material, the process comprising steps of:

formatting of etched layers on the active layer;

bonding the wafer by its front face onto a support substrate;

and thereafter thinning down of the semiconductor wafer via a backside opposite the front face, depositing at least one metal layer on the backside thus thinned, and etching at least one contact pad in said metal layer,

said process including the following steps :

etching narrow trenches into the thin active layer, before the bonding operation, these trenches extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation,

filling the space opened by said trenches with a conducting material isolated from the active layer, thus forming conducting vias between the front face and the backside of the thinned wafer,

wherein said trenches comprise a continuous trench completely surrounding a semiconductor region below said contact pad, the contact pad being electrically connected through said semiconductor region to at least one conductive layer formed during said step of formatting, and the contact pad being isolated from the conductive material filling said continuous trench.

32. (New) The process as claimed in claim 31, wherein the trenches are formed before other deposition and etching steps of electrically functional layers on the front face of the semiconductor wafer.

33. (New) The process as claimed in claim 31, wherein said trenches comprise at least one trench in the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face.

34. (New) The process as claimed in claim 31, wherein said at least one metal layer is deposited onto the backside of the wafer after thinning, this layer being connected, by conducting vias formed within at least one narrow trench, to at least one conducting layer formed, prior to bonding the wafer onto the support substrate, on the front face of the wafer.

35. (New) The process as claimed in claim 31, wherein said electronic chips comprise at least one image sensor with a matrix of pixels and the said at least one metal layer comprises a pattern within the matrix of pixels.

36. (New) The process as claimed in claim 31, wherein layers of color filters are deposited onto the backside of the wafer after bonding and thinning.

37. (New) The process as claimed in claim 36, wherein, after deposition of the color filters, the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated.

38. (New) The process as claimed in claim 31, wherein the trenches have their internal walls coated with thin silicon oxide and are filled with polycrystalline silicon that is highly doped so as to be conducting.

39. (New) The process as claimed in claim 31, wherein the semiconductor wafer comprises a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.